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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,866	01/11/2005	Guillaume De Cremoux	NL 020624	4457

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
BEHM, HARRY RAYMOND	
ART UNIT	**PAPER NUMBER**
2838	

NOTIFICATION DATE	DELIVERY MODE
12/14/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/520,866	DE CREMOUX, GUILLAUME	
	Examiner	Art Unit	
	Harry Behm	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-12 and 16* is/are rejected.

7)☒ Claim(s) *4,13-15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 June 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

The finality of the last Office action, sent 3/14/07, is withdrawn due to the new grounds of rejection for claims 1-3 and 5-16. This office action replaces the prior office action sent 3/14/07.

The period for reply has been reset and a new shortened statutory period shall take effect from the mailing date of this action.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 9/30/05 was considered on 10/6/06. Prosecution has been reopened with a new examiner, therefore the information disclosure statement is being considered by the examiner.

Response to Arguments

Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the output terminal connected between the amplifying element and the current sensor, as in Claim 6, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 5 and 6 are objected to because of the following informalities: "the node" lacks antecedent basis. Appropriate correction is requested.

Claims 7, 8, 10, 12 and 17 are objected to because of the following informalities: the phrase "preferably a MOSFET" renders the claim unclear whether the limitation(s) in the phrase are part of the claimed invention. See MPEP § 2173.05(d). Appropriate correction is required.

Claim 9 is objected to because of the following informalities: "the second transistor" lacks antecedent basis. Appropriate correction is required.

Claims 12-13 are objected to because of the following informalities: "the comparator" lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 10 and 16 rejected under 35 U.S.C. 102(e) as being anticipated by Gang (US 6,750,638).

With respect to Claim 1, Gang discloses a capacitive feedback circuit, comprising: a voltage input terminal (Fig. 2 19); a current output terminal (Fig. 2 node C1-R1); a feedback capacitor (Fig. 2 C1), having a first terminal connected to input terminal and having a second terminal connected to a high-impedance node (Fig. 2 24 inverting input).

With respect to Claim 2, Gang discloses a capacitive feedback circuit according to claim 1, further comprising: an amplifying element (Fig. 2 24) having a high-impedance control terminal [inverting] connected to said node; a current sensor (Fig. 2

23,R1) connected in series between said amplifying element (Fig. 2 12) and a first supply voltage (Fig. 2 18); a bias current source [differential amplifier 24 has bias current, must have bias source] connected in series between said amplifying element and a second supply voltage [supply for 24].

With respect to Claim 3, Gang discloses a capacitive feedback circuit according to claim 2, wherein said current sensor (Fig. 2 33,R1) is part of a current-to-voltage converting feedback loop, which has a high-impedance output terminal connected to said node.

With respect to Claim 6, Gang discloses a capacitive feedback circuit according to claim 2, wherein the output terminal (Fig. 2 node R1-C1) is connected to the node between the amplifying element (Fig. 2 24) and the current sensor (Fig. 2 33).

With respect to Claim 10, Gang discloses a capacitive feedback circuit according to claim 2, wherein the current sensor comprises a combination of two transistors (current mirror 33 must have at least two transistors), preferably MOSFETs, connected in a current mirror (Fig. 2 33) configuration.

With respect to Claim 16, Gang discloses a voltage regulator (Fig. 2 20) comprising a capacitive feedback circuit according to claim 1.

Claims 1-2, 5, 7-8 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Summe (US 5,289,109).

With respect to Claim 1, Summe discloses a capacitive feedback circuit, comprising: a voltage input terminal (32); a current output terminal (84); a feedback

capacitor (85), having a first terminal connected to input terminal and having a second terminal connected to a high-impedance node (26).

With respect to Claim 2, Summe discloses a capacitive feedback circuit according to claim 1, further comprising: an amplifying element (24) having a high-impedance control terminal (26) connected to said node; a current sensor (22) connected in series between said amplifying element (24) and a first supply voltage (18); a bias current source (38) connected in series between said amplifying element (24) and a second supply voltage (10).

With respect to Claim 5, Summe discloses a capacitive feedback circuit according to claim 2, wherein the output terminal (84) is connected to the node between the amplifying element (24) and the bias current source (alternately 46 can be view as the bias current source and GND as the second supply voltage).

With respect to Claim 7, Summe discloses a capacitive feedback circuit according to claim 2, wherein the amplifying element (24) comprises a first transistor (24), preferably a MOSFET, having its gate (26) connected to said node.

With respect to Claim 8, Summe discloses a capacitive feedback circuit according to claim 2, wherein the bias current source (38) comprises a second transistor (38), preferably a MOSFET, having its source (12) connected to second supply voltage (10), and having its gate connected to a source (52) of accurate constant bias voltage.

With respect to Claim 16, Summe discloses a voltage regulator (12-88) comprising a capacitive feedback circuit according to claim 1.

Claims 1-2, 10, 12 and 16 rejected under 35 U.S.C. 102(b) as being anticipated by Edwards (US 5,637,992).

With respect to Claim 1, Edwards discloses a capacitive feedback circuit, comprising: a voltage input terminal (Fig. 2 node 44-45); a current output terminal (Fig. 2 node 40-44); a feedback capacitor (Fig. 2 44), having a first terminal connected to input terminal and having a second terminal connected to a high-impedance node (Fig. 2 40-44).

With respect to Claim 2, Edwards discloses a capacitive feedback circuit according to claim 1, further comprising: an amplifying element (Fig. 2 40) having a high-impedance control terminal connected to said node; a current sensor (Fig. 2 38) connected in series between said amplifying element and a first supply voltage (Fig. 2 VDD); a bias current source (Fig. 2 42) connected in series between said amplifying element (Fig. 2 40) and a second supply voltage (Fig. 2 GND).

With respect to Claim 10, Edwards discloses a capacitive feedback circuit according to claim 2, wherein the current sensor (Fig. 2 38, 50) comprises a combination of two transistors, preferably MOSFETs, connected in a current mirror configuration.

With respect to Claim 12, Edwards discloses a capacitive feedback circuit according to claim 2, wherein the comparator comprises a combination of two transistors (Fig. 2 38,50) , preferably MOSFETs, connected in a current mirror configuration.

With respect to Claim 16, Edwards discloses a voltage regulator (Fig. 2 60) comprising a capacitive feedback circuit according to claim 1.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards (US 5,637,992) in view of Sedra.

With respect to Claim 7, Edwards discloses a capacitive feedback circuit according to claim 2, wherein the amplifying element comprises a first transistor (Fig. 2 40), having its base connected to said node (Fig. 2 40-44). Edwards does not disclose MOSFETs for the differential pair 36,40. Sedra teaches using a MOSFET differential pair (Fig. 6.29 Q1,Q2). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a MOSFET differential pair. The reason for doing so is "compared to BJTs, MOS transistors can be made quite small (that is occupying a small silicon area) and their manufacturing process is relatively simple", Sedra page 299).

With respect to Claim 8, Edwards discloses a capacitive feedback circuit as set forth above. While Edwards does not disclose the structure of the current source (Fig. 2 42), it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the bias current source comprises (Fig. 2 42) with a second

transistor (Sedra Fig. 6.32 Q2), preferably a MOSFET, having its source connected to second supply voltage [-Vss], and having its gate connected to a source of accurate constant bias voltage [Iref]. The reason for doing so is "current mirrors are used in the design of currents sources for biasing" (Sedra page 453).

With respect to Claim 9, Edwards in view of Sedra discloses a capacitive feedback circuit according to claim 7, wherein the second transistor (Fig. 6.32 Q2) has its drain connected to the source of the first transistor (Fig. 2 40).

With respect to Claim 11, Edwards in view of Sedra discloses a capacitive feedback circuit according to claim 7, wherein the current sensor comprises a third transistor (Fig. 2 38) having its source connected to first supply voltage (Fig. 2 VDD) and having its drain connected to the drain of the first transistor (Fig. 2 40), and further comprises a fourth transistor (Fig. 2 50) having its source connected to first supply voltage (Fig. 2 VDD) and having its gate connected to the gate and to the drain of the third transistor (Fig. 2 38).

Allowable Subject Matter

Claims 4, 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if any objections stated above are overcome.

With respect to Claim 4, the following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, having a

second input connected to receive a reference current, and having a voltage output connected to said node.

With respect to Claims 13-15, the following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, wherein a sixth transistor having its gate connected to the gate and to the drain of the fifth transistor.

Claim 17 would be allowable if the objections stated above are overcome.

With respect to Claim 17, the following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose or suggest, in combination with the limitations of the base claim and any intervening claims, primarily, wherein one transistor has its drain connected to receive said sensor output current signal and wherein the other transistor has its drain connected to the source of the input transistor.

The aforementioned limitations in combination with all remaining limitations of the respective claims are believed to render the aforementioned indicated claim and any dependent claims thereof patentable over the art of record.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on 7:00 am - 3:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on (571) 272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey Sterrett
Primary Examiner